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Shijia Wei

Ph.D. Student working in Computer Architecture and Security

Education

August 2016 – May 2021 **The University of Texas at Austin**, *Department of Electrical and Computer Engineering*
Ph.D. in Architecture, Computer Systems, and Embedded Systems.

September 2015 – May 2016 **Harvard University**, *Harvard School of Engineering and Applied Sciences*
Undergraduate Overseas Research Fellow, Ministry of Education of China.

September 2013 – June 2016 **Zhejiang University**, *Qizhen Honors Class, Chu Kochen Honors College*
B.Eng in Computer Science.

Research Experience

August 2016 – Present **Spark Research Lab, The University of Texas at Austin**,
Graduate Research Assistant, Advisor: Prof. Mohit Tiwari.

Cyclone: Detecting μ-architectural information leaks through cyclic interference

- An tagged architecture that supports software-defined domains to meet application-level security requirements: mutually distrusting security domains usually outnumber core, process, and VM counts.
- Implemneted in the Gem5 OoO ARMv8 full system simulation to statistically track cyclic interference.
- Perfectly detecting cache covert-channels and Spectre.js with orders of magnitude lower false positives.

Detecting Microarchitectural Attacks using Power-Trace in Embedded/IoT Systems

- Power sensors are always available in most of the embedded devices. Power traces of a running system provide a analog view of the system which suggests a feasible and promising out-of-band method to detect damaging microarchitectural attacks.
- Attacks that use microarchitectural resources to escalate privileges and leak secrets have elicited extensive attack-centric defenses. I evaluated power-based machine learning detector against both baseline and evasive rowhammer and cache/memory-based covert channel attcks.

May 2017 – August 2017 **AMD Research**,
Co-Op Engineer, Mentor: Dr. Joseph Greathouse.

Instruction-Level Power Model for x86

- AMD Instruction-Based-Sampling (IBS) provides details of most frequent instructions of running applications as well as microarchitectural events associated with them. With IBS, we design a power model that decouples instruction baseline energy cost from energy burned by microarchitectural events.
- Providing detailed instruction-level power model to software developers and compilers helps them designing, debugging energy-efficient and power side-channel free software.

September 2015 – May 2016 **The Data Systems Laboratory, Harvard University**,
Undergraduate Researcher, Advisor: Prof. Stratos Idreos.

Workload Aware Data Partitioning for Hybrid Analytics

- Exploring trade-off of modern access methods between read, update performance and memory overheads helps with designing better data systems for hybrid analytic workloads.
- Adaptive decisions on partitioning properties like size and number of partitions based on the workload requirements and the hardware characteristics gives the system a balanced overhead and perforamce, achieving better overall latency and throughput.

May 2015 – August 2015 **Computer Architecture Laboratory, Zhejiang University**,
Research Assistant, Advisor Prof. Wenzhi Chen.

Non-volatile memory NAND-Flash Emulator on FPGA

- Integrated PCIe Endpoint specification IP On FPGA.
- Implemented NVMe protocol Decode and Control Logic.

Selected Projects

Memcache-SGXd — Evaluated different porting schemes to secure Memcached in SGX per various threat models. Explored optimizations like dedicated syscall thread, reducing boundary crossing, and libOS.

Cache Replcement Policy — Designed an I-Cache replacement policy based on run-time basic block signatures, improving performance of server workload for Node.js apps–**I-Cache MPKI reduced by up to** 7×;

FPGA, GPU Performance — Performance study using Cuda for GPU and OpenCL for FPGA for embarrassingly parallel applications like matrix-multiplication, bloom filter, and single-source-shortest-path.

Zynq GO — A FPGA-ARM based system that employs Zynq-linux and GNUGO running a online *GO* game.

Pascal Compiler — Led a team of four undergraduates to design and develop a compiler that compiles Pascal to x86 assembly, explored static optimizations.

Teaching and Voluntary

Spring 2017 — **Teaching Assistant**, *Introduction to Embedded Systems, The University of Texas at Austin.* With Prof. Mohit Tiwari and Prof. Jonathan Valvano

February 2017 — **Volunteer**, *HPCA/CGO/PPoPP 2017*, Austin, TX.

Fall 2016 — **Teaching Assistant**, *Real-Time Bluetooth Networks (edX), The University of Texas at Austin.* With Prof. Jonathan Valvano and Dr. Ramesh Yerraballi

Summer 2015 — **Head Teaching Assistant**, *Introduction to Computing Systems, Zhejiang University.* With Prof. Yale N. Patt at and Prof. Xiaohong Jiang

September 2014 — **Volunteer**, *VLDB 2014*, Hangzhou, China.

Summer 2014 — **Teaching Assistant**, *Computer Organization, Zhejiang University.* With Prof. Yamin Lee and Prof. Qingsong Shi

Skills and Languages

- Gem5, SniperSim, PINTool
- C/C++, Shell, Python, Pascal, Java
- Pratical Verilog and Chisel
- Proficient English, Native Chinese
- AMD IBS, perftools, PAPI, and vtune
- CUDA and OpenMP
- Git, GNU Autotools, and Latex