Shijia Wei
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Education

- **The University of Texas at Austin** — Austin, TX
  Ph.D. in Architecture, Computer Systems, and Embedded Systems (ACSES), Dept. of ECE — *August 2016 – May 2021*
  TA for *Introduction to Embedded System*, and *Real-Time Operating Systems* with Prof. Jonathan Valvano.
- **Harvard University** — Cambridge, MA
  Undergraduate Overseas Research Fellowship, Ministry of Education of China — *September 2015 – May 2016*
- **Zhejiang University** — Zhejiang, China
  B.Eng. in Computer Science, Chu kochen Honors College — *October 2012 – June 2016*
  Head TA for *Introduction to Computing Systems* with Prof. Yale Patt.

Research

- **Spark Research Lab, The University of Texas at Austin** — Austin, TX
  Graduate Research Assistant, Advisor: Prof. Mohit Tiwari — *August 2016 - Present*
  - **Cyclone**: Detecting micro-architectural information leaks through cyclic interference. (Lead author, submitted to **ISCA'19**)
    - Evaluated Cyclone using Gem5 OoO ARMv8 full system simulator and modified PhantomJS (WebKit) to label JS origins as security domains
    - Cyclone detects prime+probe cache attacks and Spectre.js with orders of magnitude lower false positive rate relative to using best-known prior work (that track performance counters or contention alone).
  - **Power-Anomaly**: Detecting micro-architectural attacks in embedded systems as power-channel anomalies. (Lead author, submitted to **HOST'19**)
    - Developed an algorithm to construct evasive micro-architectural covert-channels, speculation-drive attacks, and Rowhammer that mimic the power signatures of a benign application.
    - Evaluated machine learning algorithms like SVM, LSTM, and xgBoost on power-traces to detect evasive attacks hidden in OpenCV, ROS, encryption, and compression programs.
  - **Lean Stack**: Accelerator architecture for serverless applications
    - Programmable accelerator in-line with network traffic to offload application-layer routing and functions.
    - Implemented using Chisel on an x86-FPGA server, and evaluated on Memcached, ELK Stack, etc.
- **AMD Research** — Austin, TX
  Co-op Engineer, Mentor: Dr. Joseph Greathouse — *May 2017 - August 2017*
  - **Parallel Optimization**: Contributed to the AMD Research Instruction-Based-Sampling (IBS) Toolkit.
    - Developed a parallel tool that automates annotation of hot code path for IBS Toolkit.
  - **x86 Instruction-level Power Model**: A methodology for instruction power modeling with IBS (Patent filed).
    - Developed a power model that decouples instruction baseline power from micro-architectural events power.
- **DASlab, Harvard University** — Cambridge, MA
  Undergraduate Researcher, Advisor: Prof. Stratos Idreos — *September 2015 - May 2016*
  - **Workload-Aware Column-Store**: Heuristic based range partitioning for column store data systems
    - Developed a novel range partitioning scheme to trade-offs between read-/update-latency, and memory overhead.

Selected Class Projects

- **Memcache-SGXd**: Evaluated different porting schemes (e.g. SCONE, partitioning) to secure Memcached in SGX for various threat models. Evaluated optimization schemes like dedicated syscall thread and reducing boundary crossing.
- **I-Cache Replacement Policy**: Developed an I-cache replacement policy using run-time basic block characteristics, improving server workload performance for Node.js apps—**I-Cache miss rate (MPKI) reduced by up to** 7×.
- **Performance Evaluation between FPGA and GPU**: Performance study using, Cuda, OpenCL for GPU and FPGA, on embarrassingly parallel applications like matrix-multiplication, bloom filter, and single-source-shortest-path.
- **Remote Attacks on ARM**: Implemented Rowhammer, AnC, and Spectre in JavaScript.

Skills

Languages C/C++, Python, Bash, x86/ARM Assembly, Java, Verilog
Tools Gem5, SniperSim, PINTool, AMD IBS, PAPI, Perftools, VTune, Autotools